IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Marina V. Plat and Angela T. Hui
Serial No.:	10/079,775
Filed:	February 19, 2002
Title:	METHOD & SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST
Art Unit:	2823
Examiner:	Lee, Hsien Ming

DECLARATION PURSUANT TO 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Dear Sir:

I, Marina V. Plat declare that:

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 11-4, 2003.

Toni Stanley
Signature

Toni Stanley
(Printed name of person certifying)

1. I am a joint inventor of the subject matter of the present U.S. patent application, Serial No. 10/079,775, METHOD & SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST filed on February 19, 2002, with a first priority date of November 2, 1999.

2. I have been informed that in the present application, certain claims have been rejected based in part on a reference to Chung et al. (U.S. Patent No. 6,184,142) (hereinafter "*Chung*"), Serial No. 09/302,204, entitled "Process for Low K Organic Dielectric Film Etch" with a priority date of April 26, 1999 and in part on a reference to Li, et al. (U.S. Patent No. 6,423,628) (hereinafter "*Li*"), Serial No. 09/425,552, entitled "Method of Forming an Integrated Circuit Structure Having Low Dielectric Constant Material and Having Silicon Oxynitride Caps Over Closely Spaced Apart Metal Lines" with a priority date of October 22, 1999.

3. As set out in detail below in paragraphs 5-7, my co-inventor and I conceived of the subject matter claimed in the present invention within the United States prior to the effective dates of Chung and Li.

4. As set out in detail below in paragraphs 8-11, beginning from a date earlier than the effective dates of Chung and Li, my co-inventor and I diligently pursued reduction to practice of the invention through the filing of the present application.

CONCEPTION

5. Exhibit 1, attached hereto, is a true copy of a disclosure of the present invention as submitted to counsel during an invention harvesting session at Advanced Micro Devices, Inc. ("AMD").

6. Page number 2 of Exhibit 1 describes the problem with the prior art semiconductor fabrication process. The disclosure also provides a solution to the problem. The disclosure provides evidence that the claimed method for reducing removal of the antireflective-coating (ARC) layer during removal of a photoresist layer during semiconductor fabrication was conceived at the time of the patent harvesting session.

7. The date of the disclosure in Exhibit 1 has been redacted; however, the date of the disclosure predates the effective date of the *Chung* and *Li* patents.

REDUCTION TO PRACTICE

8. On information and belief, my co-inventor and I were diligent in constructively reducing our invention to practice through the preparation and filing of a patent application that described and claimed the subject matter of our invention.

9. During a period beginning prior to the effective date of the prior art references we worked with counsel on the preparation of a patent application describing and claiming the subject matter of our invention. Attached as Exhibit 2 are copies of letters from counsel forwarding draft copies of the application for review.

ATTORNEY DOCKET NO.PATENT
D900DU.S. Serial No. 10/079,775

10. Said application was executed by my co-inventor and I, and filed with the United States Patent and Trademark Office on or about November 2, 1999. The application was assigned Serial No. 09/433,541.

11. The present application is a divisional of application Serial No. 09/433,541 and claims priority from that application.

12. I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application of any patent issued thereon.

Marina V. Plat — 10.23.03

Marina V. Plat — Date

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Angela T. Hui, declare that:

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Angela T. Hui

10/07/03
Date

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184-P057D1

OCT-07-2003 TUE 05:50 PM AMD FAX NO. 408 749 5144 P. 02

CS59|CDR3-Group3 - Room C-3 NDR PROCESSES (A) CORE JUNCTION|SAS

AMD INVENTION DISCLOSURE TLD ID# D960 Rec'd date _____

Sunnyvale x42110, return to MS 68. Texas x55964 return to MS 562

*********user see Readme.doc********

3-9

Project: ☐, **Product:** ☐, **Process:** ☐, **Technology** ☐, **to which the invention applies (*identify*):** _____

List 2 to 5 key words useful to search by to find patents or art related to this invention: SiON depletion, multireflective coating, Strip Resist procedure

Working title of invention: Change in the resist strip procedure after Implant steps to minimize SiON ARC thickness depletion

(Inventor/participant information is on next page)

Inventor's signature : _____ **date :** _____

Inventor's printed full name: ~~MARINA PLAT~~ Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone:( ) _____

Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

Co-Inventor's signature : Angela Hui date : _____

Co-Inventor's printed full name: _____ Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone:( ) _____

Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

Co-Inventor's signature : _____ date : _____

Co-Inventor's printed full name: _____ Citizenship: _____

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Post Office address: _____

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Division: _____ Directorate: _____ Dept #: _____ Dept : _____ Manager: _____

Residence address: _____

Post Office address: _____

List on additional sheet if there are more co-inventors and list total number of inventors here: _____

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known: Arthur Steiner MWE

Witness 1 initial: _____ Witness 2 initial: _____

Exhibit 1

AMD INVENTION DISCLOSURE TLD ID#_____ Rec'd date_____
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

Identify known relevant art (patents, publications, products): _____

State the problem solved by this invention: SiON thickness depletion by wet due to wet resist strip procedures
Thickness loss will cause increased line width variation and Reflective notching

Brief description and/or sketch of invention (*please attach copies of AMD patent notebook pages, reports or drawings*): SDR-3 - process flow: for 2-nd Gate
1. Stacked gate poly dep and SiON deposition.
2. Stacked gate poly etch and resist strip #1
3. Implants 5-6 masking steps require resist strip
4. 2Gate masking - effected due to eroded ARC thickness

Problem: 10-20A SiON loss after every wet resist strip.
wet resist strip is needed ~~At~~ Stack gate and 2GM
Masking steps to prevent ~~xx~~ residual poly defects
Potential SiON loss during step 1-4 60-~~1~~00A.
Result: CD variation and reflective notching.

Solution: Implement dry etch Resist strip at step 3
using 4% ~~for~~ forming gas plasma strip, which will
minimize SiON depletion and 2GM rem
Use wet precleam prior to ~~Rich~~ 2GM. to
minimize defects.

Patent notebook # _____ Page numbers_____ Number of drawings_____

Witness 1 initial: _____ Witness 2 initial: _____